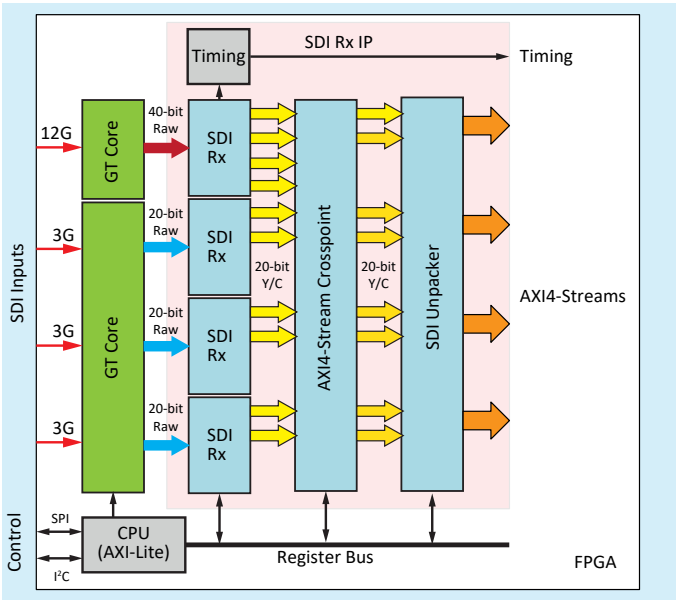
SDI
Xilinx FPGA IP

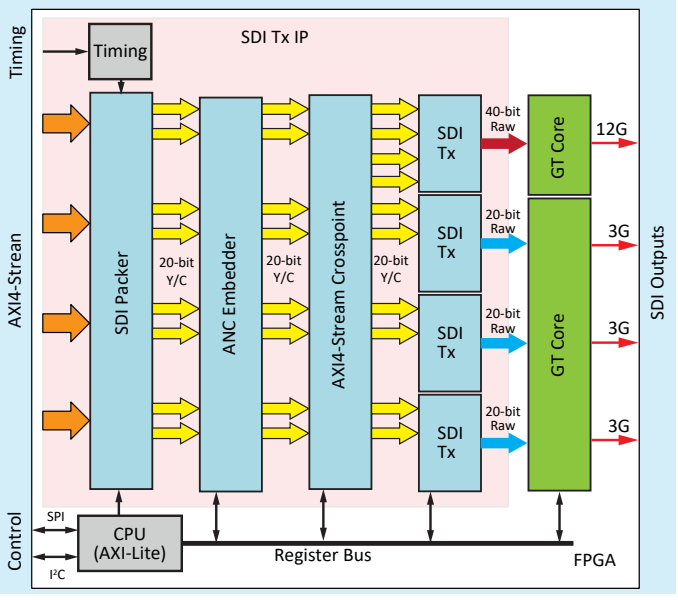
Omnitek

Summary

The Omnitek SDI IP is a highly optimised Xilinx FPGA IP Core to allow the conversion of any SMPTE Serial Digital Interface video data stream into an AXI4-Stream with support for single link (up to 12G-SDI), dual link (up to 6G-SDI) and quad link (3G-SDI). This IP comes as independent Rx and Tx IP. The Rx IP decodes an SDI video stream into a neutral AXI4-Stream and the Tx IP encodes a neutral AXI4-Stream into the chosen SDI video stream format.



Functional block diagram of the SDI Rx IP



Functional block diagram of the SDI Tx IP

Omnitek provides a large range of complementary IP Cores for video processing and connection. These IP cores can be used individually or in combination to provide FPGA solutions for applications in broadcast, AV, aerospace/defence, medical and automotive industries. Omnitek IP Cores can be supplied as discrete blocks for inclusion in your own designs, as single chip solutions or Omnitek can provide a bespoke solution which can be tailored to your specific needs.

Key Features

- Very small FPGA resource footprint
- Multichannel GT-SDI support
- 5-Rate 12G Fully loaded Gate Count, 70% smaller than Xilinx
- Over 1700 SMPTE SDI Video standards supported
- Both 4K Square Division and 2 Sample Interleave Processing
- SD-SDI, HD-SDI, 3G-SDI, 6G-SDI and 12G-SDI support
- Independent Rx/Tx IP
- Output of active video and full raster video with blanking
- Audio Extraction and Embedding
- SMPTE 352 Packet Extraction and Embedding
- Loop-back test mode
- Bare Metal and Linux Support Libraries

Applications

The SDI Core can be used in a range of applications including:

- SDI Input / Output connection for broadcast equipment
- SDI Input for high end projectors
- SDI to HDMI conversion
- SDI to V-by-One conversion
- Gearbox from one SDI format to another
- Video Standards conversion

Example Resource Usage

The total resource count will depend on the chosen implementation. The SDI Rx and Tx IP typically use the following resources based on the Xilinx Kintex 7-series devices:

IP Core	Configuration	Registers / Flip Flops	LUTs	Block RAM
GT	1 Rx/Tx Pair	812	700	2
GT	4 Rx/Tx Pairs	3312	2345	8
SDI-Rx	Triple Rate	1000	1800	1
SDI-Rx	5 rate	1300	2300	1
SDI-Tx	Triple Rate	400	300	
SDI-Tx	5 Rate	440	340	
SDI Unpacker	Triple Rate	800	700	
	5 rate level-A only	3123	2000	12
	5 rate all standards	4597	3103	24
SDI Packer	Triple Rate	800	850	
	5 rate level-A only	2400	4800	12
	5 rate all standards	5800	3800	24
Timing				
AXI4-S Crosspoint				

Additional Requirements

The SDI IP requires an ARM processor, MicroBlaze or any AXI4-Lite CPU to allow configuration of the input link selection, SMPTE format detection and output configuration.

IP Sub Blocks

The SDI IP consists of the following elements:

The "**GT Cores**" are used to perform 20bit parallel to/from serial conversion. This is shared by the RX & TX IP. Note that (just) this core could be exchanged for a GTH (or other) version for adaptation to other Xilinx FPGA families.

The "**SDI Rx**" blocks are used to perform standard detection and extract a decodable 20bit YC SDI stream or pixels from raw GT data.

The "**SDI Unpacker**" is used to perform Y/C stream decoding into true pixel data.

The "**SDI Tx**" blocks are used to perform stream gear-boxing (same frame rate conversion between different video link structures) and final 20bit encoding ready for serialisation by a GT Core.

The "**SDI Packer**" is used to encode true pixels into SDI Y/C streams and merge video timing.

The "**Timing**" block is used to generate output video timing for any interface.

The "**AXI4_Stream Crosspoint**" is a software controlled generic AXI4S crosspoint with built in CDC (clock domain crossing).

SDI Video Input / Output Formats (SMPTE)

The SDI IP can process video formats up to 4K @60 Hz frame rate:

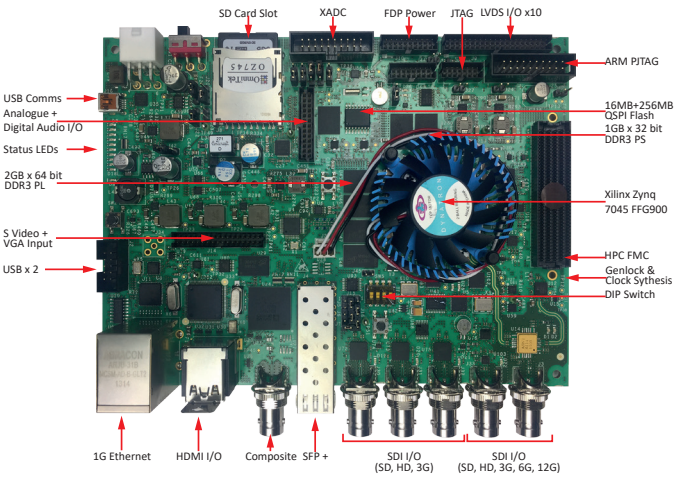
4096x2160p	23.98/24/25/29.97/30/47.952/48/50/59.94/60Hz
3840x2160p	23.98/24/25/29.97/30/50/59.94/60Hz
2048x1080p	23.98/24/25/29.97/30/47.952/48/50/59.94/60Hz
1920x1080p	23.98/24/25/29.97/30/50/59.94/60Hz
2048, 1920x1080sF	23.98/24/25/29.97/30Hz
2048, 1920x1080i	50/59.94/60Hz
1280x720p	23.98/24/25/29.97/30/50/59.94/60Hz
720x486i	59.94, 576i - 50Hz
UHDTV1 50/60	12G-SDI ST 2082-10 (2SI) Dual-link 6G-SDI ST 2081-11 (2SI) Quad-link 3GA-SDI/3GB-SDI ST 425-5 (2SI and SQ)
UHDTV1 25/30	6G-SDI ST 2081-10 (2SI) Dual-link 3GB-SDI ST 425-3 (2SI and SQ) Quad-link HD-SDI (SQ)
HD 1080p	3GA-SDI/3GB-SDI/3GB-DS-SDI/Dual-link HD-SDI ST 425-1, 372
HD/SD	HD-SDI/SD-SDI ST 2048-2, 274, 296, 259 2SI = 2 Sample Interleaved, SQ = Square Division
Sampling	4:2:2, 4:4:4 Y'Cb'Cr', R'G'B', X'Y'Z' : 8, 10, 12 bits
Colour spaces	EBU (ITU-R BT.470 standardized RGB), ITU-R BT.601, ITU-R BT.709, ITU-R BT.2020, DCI (SMPTE RP 431), SMPTE C (SMPTE RP 145)

RTVE Reference Design

Xilinx's RTVE reference design (Real-Time Video Engine) incorporates a range of IP cores alongside the OSVP Suite (Omnitek Scalable Video Processor) to provide video processing IP and connectivity IP functionality that offers a complete working FPGA design that can be used both to evaluate the performance of the IP blocks in a video application and as a starting point for your own video system designs.

Reference Platform

The Omnitek OZ745-3 development platform uses the Xilinx Zynq-XC7Z045-3



Supported Devices

The SDI IP can be implemented on the following devices:

- Artix-7, Kintex-7 and Virtex-7
- Kintex UltraScale and Virtex UltraScale
- Kintex UltraScale+ and Virtex UltraScale+
- Zynq-7000 APSoC and Zynq UltraScale+ MPSoC

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About Omnitek

Omnitek is a leading independent consultancy company specializing in the design of products and IP for the broadcast, post-production, digital film, AV, medical, aerospace/defence, automotive and consumer industries. Since its foundation, Omnitek has completed many successful design projects for major equipment manufacturers throughout Europe, Asia, and the United States.

Omnitek reserves the right to change specifications without notice. Refer to the Omnitek web site for the latest specifications and further information:

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