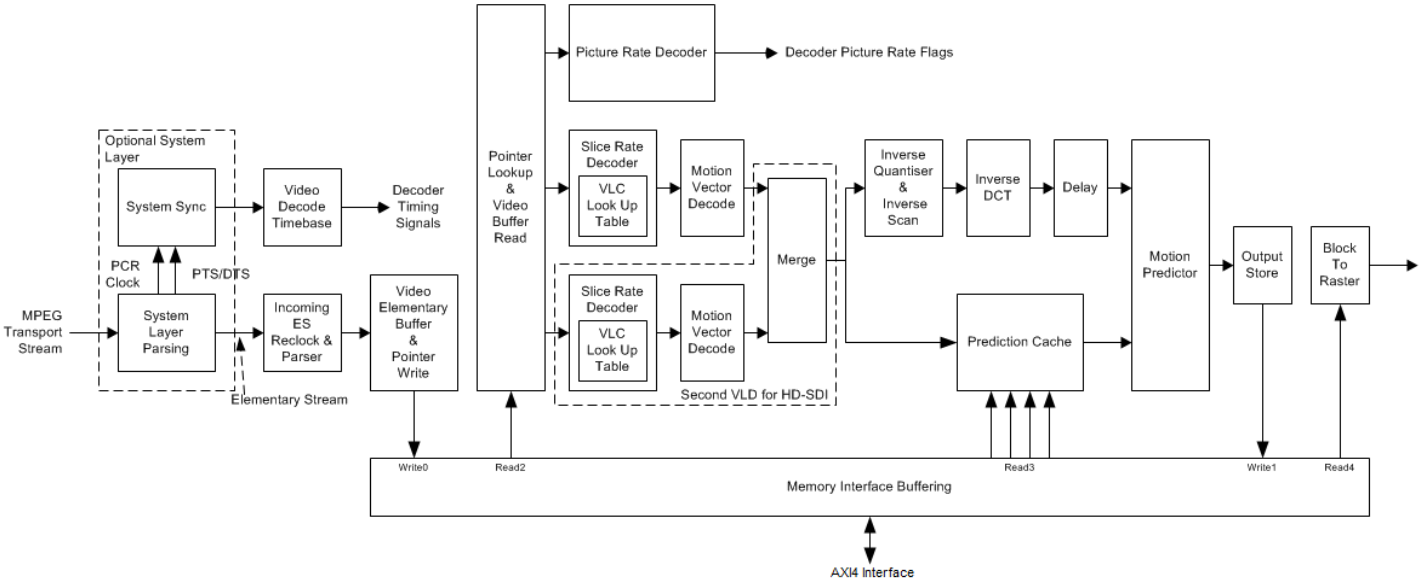
MPEG2 Video Decoder Xilinx IP Core

OmniTek

Meeting requirements of the 13818-4 conformance specification, including the requirement to decode ‘constrained parameter’ MPEG1.



Key Features

- Professional MPEG2 Video decoder firmware for Xilinx FPGAs or alternative technologies (if required)
- 27MHz or 148.5MHz processing clock for SD and HD images respectively
- Efficient external memory interface: SD-SDI decode typically requires a single 8bit interface to DDR2 SDRAM
- Compliant to ISO13818-2 (ITU-T H.262) 4:2:2Profile@HighLevel
  - 4:2:0 and 4:2:2 format support
  - Up to 2048*1080 resolution
  - I, P and B picture support
  - Field or Frame picture structure
  - Half Pixel prediction accuracy
  - Field, Frame, 16x8 and DualPrime prediction modes
- FPGA optimised design
  - Inverse DCT optimised for embedded DSP blocks
  - Integration within Xilinx EDK design environment
  - AXI4-Lite memory and control interfaces
- Validated against ISO13818-4 conformance bit streams
- Optional ‘System Layer’ extracting timing data
- Decoder block, System Layer block and wrappers optionally available as source code in either Verilog or VHDL.
- Embedded control software for parsing SI tables available as C++ source code
- Free 30-day evaluation
- IP customisation and board development services also available

Deliverables

- Encrypted netlist or Source code for MPEG2 Decoder Core
- Software source code for parsing transport stream SI tables (Full package only)
- Project file/wrapper supporting integration with compatible FPGA components
- RTL simulation environment (Full package only)
- Pre-compiled ModelSim libraries for the encrypted parts of the MPEG video decoder (Full package only)
- Complete EDK reference design for Virtex6
- Reference design includes drivers and application for Windows® 7™ and XP™
- Comprehensive documentation
- Technical Support and Maintenance Updates

Typical resource use

	LUTs	Registers	Memory Blocks	DSP Blocks
MPEG2 Dec. (HD-SDI)	8000	6200	50	28

Reference Design

The MPEG video decoder is provided together with a working reference.

When used in a host PC, the design is able to operate either as a free-running decoder, requesting elementary stream data from the DMA controller as required, or as a transport stream decoder being passed data from an ASI interface.

The decoder is integrated inside the Xilinx EDK design environment with Xilinx's DDR2 MIG Memory Controller and MicroBlaze processor, and the OmniTek PCIe streaming DMA controller.

Licensing Options

Evaluation licence

- Available for free for 30 days through OmniTek website. Includes reference design with pre-compiled driver and application, and access to documentation (unencrypted).

Annual Encrypted IP licence

- Allows IP to be used in a production system. Pack includes all items in evaluation package plus RTL simulation environment, pre-compiled ModelSim libraries, and software for parsing SI tables

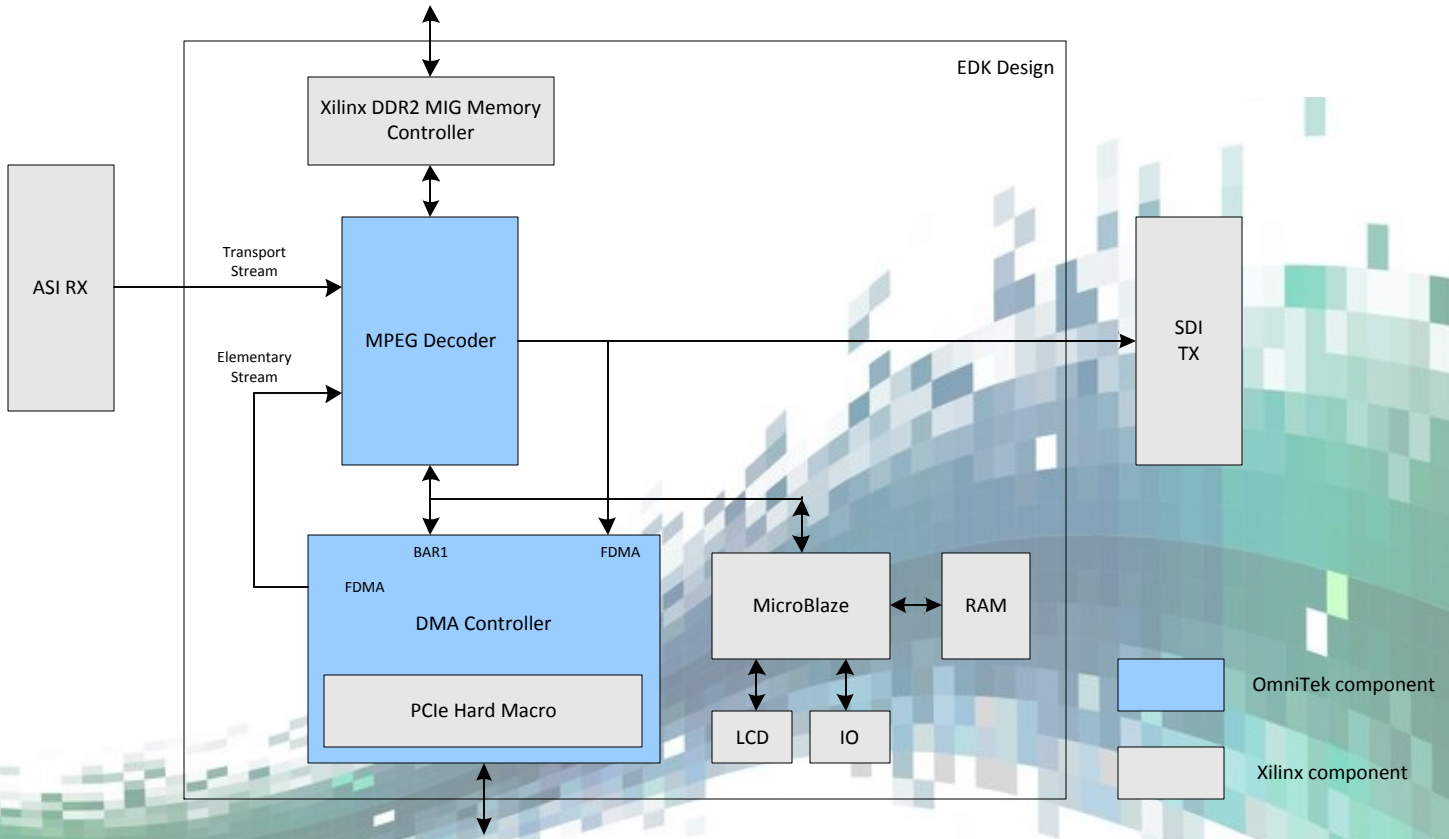
Source Code licence

- Allows customisation of IP.

Depending on the target application, additional license fees may be payable to the MPEG LA.

Product Options

- Annual Licence or Source Code
- System Layer Block
- HD Support
- FPGA family
- Extended evaluation period (over 30 days)
- Extended support period (over 1 year)



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