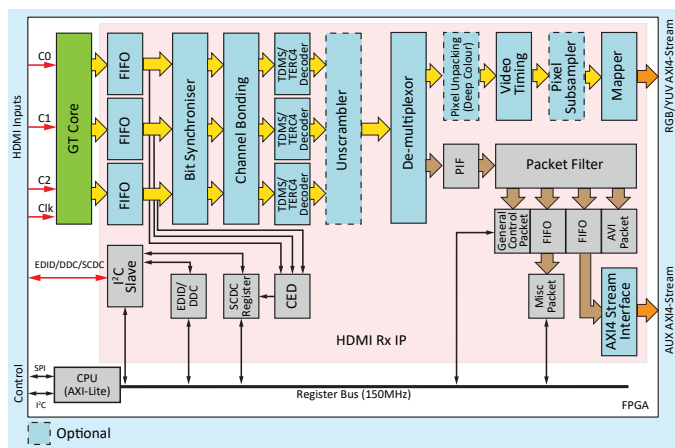


## Summary

The Omnitek HDMI IP Core consists of the HDMI Rx IP and the HDMI Tx IP. The HDMI Rx IP will convert an HDMI video stream up to 4KP60 to a RGB/YUV video AXI4-Stream and an auxiliary AXI4-Stream. The HDMI Tx IP will convert a RGB/YUV video AXI4-Stream plus AUX data AXI4-Stream to a HDMI video stream.

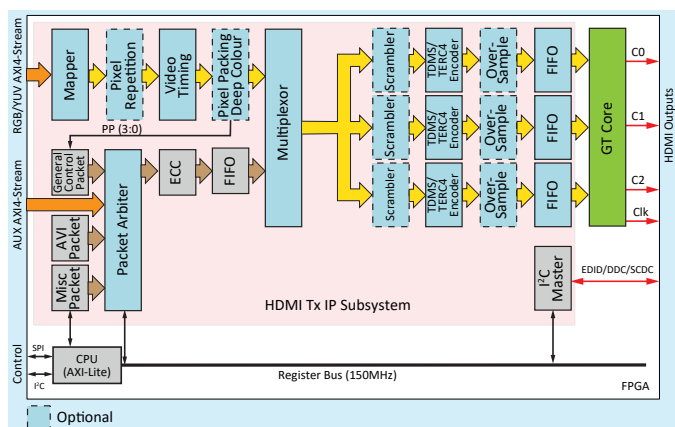
The HDMI Rx and HDMI Tx IP support HDMI 1.4 and HDMI 2.0 datastreams up to 6.0Gbps.

## HDMI Rx IP



HDMI channels are de-serialised, checked, synchronized and bonded. The data is decoded to remove the TMDS encoding then unscrambled. The unscrambled data is de-multiplexed into an RGB/YUV video stream and an auxiliary data stream. The video data stream is unpacked, timed, sub-sampled and then mapped as a RGB/YUV AXI4-Stream. The auxiliary data stream is filtered to extract different packets and output as an AXI4-Stream.

## HDMI Tx IP



RGB/YUV Video data as an AXI4-Stream is mapped, pixel repeated, timed then multiplexed with the AUX Data on a second AXI4-Stream. The RGB or YUV data stream produced is then split into separate RGB/YUV streams for output as HDMI.

The 3 identical data channels for RGB/YUV scramble the data before encoding as TMDS (Transition Minimized Differential Signalling). The data is then oversampled and buffered before being serialised to provide the HDMI output.

## Key Features

- Very small FPGA resource footprint
- Very low output latency
- Support for image sizes up to 4096 x 2160 at up to 60 fps
- Independent transceiver PHY (GT Core) to allow ease of integration into different designs and packages
- Tx and Rx available as independent IP Cores
- Configurable optional cores to minimise resource usage
- Available as reference design
- Fully compatible with other Omnitek IP Cores via AXI4-Stream

## Applications

The HDMI Rx and Tx IP can be used in a range of applications including:

- HDMI to SDI conversion up to 4KP60
- SDI to HDMI conversion up to 4KP60
- HDMI to V-by-One conversion
- Display screen interfaces
- Projector interfaces
- Multi-screen display controllers
- Interactive display systems
- HDMI switchers/routers
- HDMI to IP conversion

## Supported Devices

The SDI IP can be implemented on the following Xilinx devices:

- Artix-7, Kintex-7 and Virtex-7
- Kintex UltraScale and Virtex UltraScale
- Kintex UltraScale+ and Virtex UltraScale+
- Zynq-7000 APSoC and Zynq UltraScale+ MPSoC

## Additional Requirements

The HDMI Rx and Tx IP require an ARM processor, MicroBlaze or AXI4-Lite CPU to allow configuration and HDMI connection feed back.

To maximise signal integrity and ensure HDMI physical layer compliance, Omnitek recommends the use of external low-cost input equalizer/re-clocker and output cable driver devices for the HDMI I/O.

## HDCP Support

The Omnitek HDMI IP core does not currently support HDCP encryption. If this feature is required, Omnitek recommends the use of low-cost external HDCP decrypt/encrypt devices; please contact Omnitek for a list of compatible parts. These external parts can also function as input equalizer/re-clocker or output cable driver if necessary.

If the application requires HDCP support included as part of the FPGA IP, there are 3rd party solutions also available. Please contact Omnitek for more details.



## IP Sub Blocks

The **Omnitek GT Cores** convert between serial and parallel AXI4 data.

The **Bit Synchronizer** and **Channel Bonding** blocks on the HDMI Rx IP ensure that the data from the HDMI input is correctly timed.

The **TMDS/TERC4 Decoder** blocks on the HDMI Rx IP remove Transition Minimized Differential Signalling from the 3 data streams.

The optional **Unscrambler** block removes Tx scrambling.

The **Demultiplexer** block on the HDMI Rx IP separates the video and auxiliary data streams.

The optional **Pixel Unpacker** block on the HDMI Rx IP extracts and High Dynamic Range information provided by the HDMI Tx.

The **Video Timing** blocks ensure that the video and auxiliary data streams are correctly co-timed before output or processing.

The optional **Pixel Sub sampler** block is required when the output AXI4-Stream data bus is faster than that of the HDMI Rx IP.

On the HDMI Rx IP, the **Mapper** block assembles the data into AXI4-Stream format. On the Tx IP the **Mapper** block converts the AXI4-Stream into the format required by the Tx IP.

The **Filter** block on the Rx IP is used to extract General Control, AVI and Misc Packet from the auxiliary data stream and outputs AXI4-S.

The optional **Pixel Repetition** block is required if the AXI4-Stream data rate is slower than that of the HDMI Tx IP.

The optional **Pixel Packing** block on the HDMI Rx IP is required to support Deep Colour (ie High Dynamic Range) content.

The **Multiplexor** block on the HDMI Tx IP is used to combine the video and auxiliary data streams.

The optional **Scrambler** blocks on the Tx IP scrambles the data.

The **TMDS/TERC4 Encoder** blocks on the Tx IP encode the 3 HDMI data streams with Transition Minimized Differential Signalling.

The optional **Oversampling** block is required if the AXI4-Stream data rate is faster than that of the HDMI Rx IP.

## HDMI Video Input / Output Formats

The HDMI Rx and Tx IP can process video formats up to 4K @60 Hz frame rate.

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## RTVE Reference Design

Xilinx's RTVE reference design (Real-Time Video Engine) incorporates a range of IP cores alongside the OSVP Suite (Omnitek Scalable Video Processor) to provide video processing IP and connectivity IP functionality that offers a complete working FPGA design that can be used both to evaluate the performance of the IP blocks in a video application and as a starting point for your own video system designs.

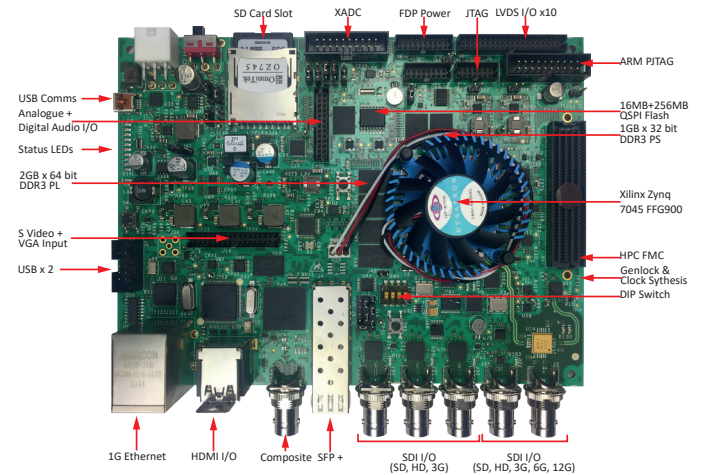


### Real Time Video Engine

Main	Warp Engine
Video Path 1	System
Input Source <a href="#">Show</a>	Board Information <a href="#">Show</a>
Cropper <a href="#">Show</a>	Test Pattern Generators <a href="#">Show</a>
Scaler General <a href="#">Show</a>	Input Connector Devices <a href="#">Show</a>
Scaler CoEff Mode <a href="#">Show</a>	Output Connector Devices <a href="#">Show</a>
Scaler Basic <a href="#">Show</a>	BiDirectional Connector Devices <a href="#">Show</a>
Scaler Sharpening V1 <a href="#">Show</a>	Overlays <a href="#">Show</a>
Scaler Sharpening V2 <a href="#">Show</a>	Output Routing & Standards <a href="#">Show</a>
Basic Colour <a href="#">Show</a>	SDI Output Chroma Downsampler <a href="#">Show</a>
6-Axis Colour <a href="#">Show</a>	Screen Layout <a href="#">Show</a>
Colour Spaces <a href="#">Show</a>	
Chroma Upsampler <a href="#">Show</a>	
Gamma Correction <a href="#">Show</a>	
OSD <a href="#">Show</a>	

## Reference Platform

The Omnitek OZ745-3 development platform using the Xilinx Zynq-XC7Z045-3 plus HDMI 2.0 FMC board are required run the RTVE 4.1 reference design supporting the HDMI Rx and Tx IP.



### About Omnitek

Omnitek is a leading independent consultancy company specializing in the design of products and IP for the broadcast, post-production, digital film, AV, medical, aerospace/defence, automotive and consumer industries. Since its foundation, Omnitek has completed many successful design projects for major equipment manufacturers throughout Europe, Asia, and the United States.

Omnitek reserves the right to change specifications without notice. Refer to the Omnitek web site for the latest specifications and further information:

[www.omnitek.tv](http://www.omnitek.tv)

