Summary

The Omnitek Projector Solution is a highly optimised FPGA IP Cores, for projectors, which provides an all-encompassing set of tools within a single design. The Projector IP can process video to create arbitrary image warps on a real time video stream of up to 4096 x 2160 pixels and at up to 60 frames per second. Maximum image quality is achieved through per-pixel filtering and bi-cubic interpolation on 4:4:4 video data at up to 10 bits per colour plane.

The Projector Solution accesses a comprehensive set of optional IP-Cores to interface to SDI, DisplayPort, HDMI, LVDS, TTL and V-by-One environments. Additional, High Quality De-interlacing, HDR (Tone-mapping) and graphics overlay IP-Cores can also be used. This flexible approach allows the Projector Solution to be implemented in the most cost effective FPGA package and allow the most effective design solutions by replacing a significant number of discrete ASIC and ASSP devices that would otherwise be needed.

Applications

The Projector Solution can be used in a range of applications including:

- DLP and LED Projectors
- 2D and 3D Projection
- Projection on to curved or distorted surfaces
- Overlay of interactive graphical and web content
- Multiple input format support, via multiple, optional, input cores
- Multiple projector installation

Key Features

- High Level Control of processing such as keystone correction, rotation, barrel and other correction, via I2C and SPI interfaces.
- GUI control via web browser interface
- Low latency (from 1 to 1/6th frame depending on transform)
- Efficient external memory interface
- Low Pass Filter coefficient sets available for adaptive filter quality
- Per-pixel low pass filtering
- Flexible design using individual IP cores such as “Warp” and “V-by-One” to suit design and component constraints.
- Optional support for image sizes up to 4096 x 2160 at frame rates up to 60 fps.
- Edge Blend with per-pixel (edge blending) control
- Optional support for SDI up to 12G, DisplayPort 1.2, HDMI 2.0, LVDS, TTL and V-by-One connections.
- Optional Interlaced video support
- Optional High Dynamic Range (Tone-mapping)
- Optional 2D Graphics Overlay
- Optional Warp Mesh Overlay

Supported Devices

The Projector Solution can be implemented on the following Xilinx devices:

- Artix-7, Kintex-7 and Virtex-7
- Kintex UltraScale and Virtex UltraScale
- Kintex UltraScale+ and Virtex UltraScale+
- Zynq-7000 APSoC and Zynq UltraScale+ MPSoC
Connectivity

Omnitek provides a large range of complementary IP Cores for video processing and connection. These IP cores can be used individually or in combination to provide FPGA solutions for applications in broadcast, AV, aerospace/defence, medical and automotive industries. Omnitek can provide a bespoke solution which can be designed for you and tailored to your specific needs.

IP Sub Blocks

Input Conditioning

The optional “SDI Rx” block provides SD-SDI, HD-SDI, 3G-SDI, 6G-SDI and 12G-SDI input connectivity to the Projector IP.

The optional “DisplayPort 1.2 Rx” block provides DisplayPort input connectivity to the Projector IP.

The optional “HDMI 2.0 Rx” block provides HDMI input connectivity to the Projector IP.

The optional “LVDS Rx” block provides a high speed communication interface with other LVDS (Low-voltage differential signalling) devices.

The optional “TTL Rx” block provides TTL input connectivity to the Projector IP.

The optional “Crosspoint” block is used when more than one Rx block is required and provides the input source switch to the Projector IP.

The optional “Chroma Resample” block is required to support 4:2:2 and 4:2:0 video formats by converting the input video into 4:4:4 format.

Image Processing

The optional “High Quality De-Interlacer” and “Scaler” blocks allow the Projector IP to support interlaced formats such as 1080i. These blocks convert the input video into progressive format. This process uses external SDRAM via the “AXI Interconnect” and “MIG” (Memory Interface Generator) blocks.

The optional “Colour Processing + Colour Correction” block allows HDR Tone-mapping to be applied to the input image.

The “Per Pixel Blend” block allows the brightness of the image to be adjusted at the edges to allow multiple projector images to be blended together. The shape and intensity of the image is controlled by the optional “Blend + Uniformity + Black Lift” block which is fed by the optional “Streaming Video DMA Processor” block.

Image Combiner

The “2D Graphics Combiner” block allows two dimensional graphics created by the optional “Linux OSD Graphics” block to be keyed over the image.

The “Warp Scaler” block manipulates the image either using high level instructions such as rotate, keystone, barrel or a mesh mapping from the “Warp load DMA” block or using a Warp mesh loaded by DMA. The input image is stored and manipulated in external SDRAM via the “AXI Interconnect” and “MIG” blocks.

The “Mesh Combiner” block combines the Warped image from the “Warp Scaler” block with a 2D Mesh Grid display from the optional “Mesh Overlay Graphics” block to create a combined image.

Output Conditioning

The optional “V-by-One Output” block allows the conversion of the output image of into V-by-One® format (2712x1528 @ 120 fps).

The optional “SDI Tx” block allows the conversion of the output image of into SD-SDI, HD-SDI, 3G-SDI, 6G-SDI or 12G-SDI format.

The optional “DisplayPort 1.2 Tx” block allows the conversion of the output image in to DisplayPort format.

The optional “HDMI 2.0 Tx” block allows the conversion of the output image in to HDMI format.

The optional “LVDS Tx” block allows the conversion of the output image in to LVDS format.

The optional “TTL Tx” block allows the conversion of the output image in to TTL format.

ARM Processor System

The Projector IP requires a processor to provide high level control and real-time update of the Warp mesh.

The Projector IP requires externally connected SDRAM. Typically a 64-bit wide @1.6GHz data rate (minimum), FFG package, 512MBytes. The ARM requires a 32 or 16-bit wide RAM @1066MHz

Omnitek FPGA chips solutions employ a pre-programmed Maxim DS28E15 512 bit EEPROM for secure authentication to enable the Omnike Projector IP.

Video Input Formats

The Projector IP can process video formats up to 4K @60 Hz frame rate (dependent on optional IP-Cores):

- SDI (SD, HD, 3G, 6G and 12G ) up to 4096x2160 resolution at 60Hz
- DisplayPort 1.2 up to 4096x2160 resolution at 60Hz
- HDMI 2.0 up to 4096x2160 resolution at 60Hz
- LVDS or TTL up to 4096x2160 resolution at 60Hz
- 10-bit, RGB, 4:4:4 processing
- 8, 10 and 12-bit, 4:2:0, 4:2:2 and 4:4:4 interface
- Up to 600MHz pixel rate
- Supports up to 4096x2160 resolution at 60Hz or 2712x1528 at 120Hz
- Support for 90° rotation of 2160x3840 input

Video Output Formats

The Projector IP can output processed video in video formats up to 4K @60Hz (dependent on optional IP-Cores):

- V-by-One® up to 4096x2160 resolution at 60Hz and 2712x1528 at 120Hz
- SDI (SD, HD, 3G, 6G and 12G) up to 4096x2160 resolution at 60Hz
- DisplayPort 1.2 up to 4096x2160 resolution at 60Hz
- HDMI 2.0 up to 4096x2160 resolution at 60Hz
- LVDS or TTL up to 4096x2160 resolution at 60Hz
- 8-bit, 10-bit or 12-bit

De-Interlacer

Interlaced and PsF format inputs need to be de-interlaced prior to signal processing. However special care is needed in order to avoid generating artefacts, particularly where the video includes motion or low-angle edges. Failure to detect film cadences correctly will also give rise to artefacts in the de-interlaced video stream.

Motion - Adaptive De-interlacing and Low - Angle Edge Correction are provided as standard and use highly-sophisticated algorithms, for Low-angle Edge Detection and Film Cadence Processing to support 3:2 and 2:2 image cadences in all video formats.
**HDR Tone-mapping (optional)**

Omnitek have developed High Dynamic Range (HDR) Tone-mapping processing techniques which dynamically adapt the processing of the ISP (Image Signal Process) data on a regional basis to enhance the overall viewing experience. This transforms a poorly lit image with little contrast into a bright image with excellent contrast.

The Omnitek HDR IP accepts RGB-format video input as an AXI4-Stream, mathematically analyses the image content and dynamically enhances the luminance range to enhance local brightness.

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**Warp Transforms**

The Warp IP, within the Projector Solution, allows the input image to be transformed using a number of controls to perform:

- Fish eye, barrel and general lens/screen distortion
- Keystone and pin-cushion correction
- Resizing and Rotation
- Perspective mapping
- Arbitrary Warps
- Edge Blending (option)

**Fixed warp transforms**

The Warp IP provides support for common transforms such as pre and post barrel / pin cushion correction and arbitrary perspective correction. These transforms can be easily configured and graphically previewed.

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**Arbitrary warp transforms**

The Warp IP also offers support for both the complete mapping of input pixels to output pixels ('Forward Grid Transformation') and / or the mapping of output pixels to input pixels ('Inverse Grid Transformation').

**Forward Grid Description**

![Forward Grid Description Diagram]

**Inverse Grid Description**

![Inverse Grid Description Diagram]

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**2D Graphics Overlay (optional)**

The image can be warped using a grid displayed as a graphical overlay. Once the desired warp has been selected the transformation of the image is completed within 0.5 of a second.

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**Picture Shape Controls**

The Warp IP determines the transformation that is needed in terms of pixel positions in the input and output. These can be set as either input or output grid values depending on the required transformation.

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3D Re-Ordering

The integrated frame synchroniser allows stereo 3D video to be delivered either as separate Left and Right image streams (in a dual pipe arrangement) or as a ‘Frame Sequential’ stream of Left and Right images.

Edge Blending core

To allow multiple projectors to be used to give a combined (or panoramic) view, an “Edge Blending” core option can be used to define regions over which the image in each projector is reduced in intensity down to black using a gamma function. This allows the resulting intensity in the overlap regions to be matched to the overall image intensity of the individual projected images.

Reference Platform

The Omnitek OZ745-3 development platform uses the Xilinx Zynq-XC7Z045-3

RTVE Reference Design

The RTVE Real-Time Video Engine 4.0 reference design incorporates the Warp IP core alongside the OSVP Suite. RTVE provides this video processing IP with connectivity IP to create a complete working FPGA design that can be used both to evaluate the performance of the IP blocks in a video application.

About Omnitek

Omnitek is a leading independent consultancy company specializing in the design of products and IP for the broadcast, post-production, digital film, AV, medical, aerospace/defence, automotive and consumer industries. Since its foundation, Omnitek has completed many successful design projects for major equipment manufacturers throughout Europe, Asia, and the United States.

Omnitek reserves the right to change specifications without notice. Refer to the Omnitek web site for the latest specifications and further information:

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