The Advanced Video Development Platform (AVDP) is a new PC-based system designed to enable video system engineers to prototype and test complex high-speed signal processing algorithms in real-time. The AVDP takes advantage of the very latest 65nm FPGA technology from Xilinx Inc. and the new high-speed PCI Express computer bus interface, to provide extremely high data processing speeds in a compact and cost-effective package.

The AVDP system has been created by Image Processing Techniques Ltd., a UK-based consultancy company providing design and development services to the TV broadcast, post-production, digital film, and image analysis industries. The company also designs and manufactures the best-selling OmniTek range of advanced test and measurement systems, for complete video and audio status monitoring.

**AVDP System Contents**
- Virtex™-5 based plug-in card with PCI Express interface & video I/O
- Comprehensive range of image processing IP, with VHDL source code
- Documented API and device drivers for Windows® XP and Vista

**Main Features**
- PCI Express x4 interface, up to 1GByte/s transfer rate
- Plug-in video interface I/O module
- 12 bidirectional serial data ports for video interfacing, up to 3.2Gbit/s each
- Accepts any Virtex™-5 device in 1136-FFG package: LX50T, LX110T, SX50T, SX95T
- 1GByte DDR-2 SDRAM clocked at 266MHz
- 144Mbit QDR-II SRAM clocked at 250MHz
- Spartan™-3 & CoolRunner™-II devices for boot control and housekeeping

**Applications**
- De-interlace and resizer algorithm development for flat-panel display devices
- High-resolution image processing for medical applications
- Development of image manipulation systems for video special effects
- Prototyping new compression codecs: MPEG-2, MPEG-4, JPEG2000 etc.
- Low-cost capture / playout card with local processing and high PC bandwidth

**AVDP Hardware Components**

**Xilinx Virtex™-5 FPGA**
The AVDP is based around the Virtex™-5 family of 65nm FPGAs from Xilinx Inc. These devices feature advanced on-chip DSP facilities, high-performance parallel SelectIO™ interface technology, and powerful on-chip clock management. The AVDP supports LXT- and SXT-series FPGAs in the 1136-FFG package, which include MGT serial transceivers with PCI Express and Ethernet hard macros. On the AVDP, the PCI Express block is configured for 1, 2, or 4 lanes of traffic, with an aggregate data bandwidth of 8Gbit/s.

**DDR2 SDRAM**
The AVDP board supports 1GByte of DDR2 SDRAM, installed as two 512MByte banks of 64bit-wide data. These are clocked at 266MHz, corresponding to a data rate of up to 533Mword/s. Note that AVDP systems fitted with the LX50T or SX50T FPGA devices only contain a single bank of SDRAM.

**QDR-II SRAM**
The AVDP system includes 4 x 36Mb QDR-II SRAM devices operating at 250MHz. These devices are burst-length-2 and are configured as 4 completely separate 2Mword x 18bit input and output busses. 72Mb or 144Mb QDR-II memory parts may also be fitted to the board, please contact OmniTek for details.

**Spartan™-3 and CoolRunner™-II Devices**
The Spartan FPGA and CoolRunner CPLD devices on the AVDP card provide various boot control operations, parallel interfacing, genlock & VCXO PLL and housekeeping functions. The Spartan device also drives an HDTV-compatible high-quality DAC for analog video output in YPbPr or RGB formats.

**Video I/O Module**
The AVDP card supports a “mezzanine” plug-in video I/O module. Connectors provide 48 high-speed parallel I/O pins plus 4 bidirectional serial links to interface with the module, and a range of different modules will be available. These include dual SDI input/output (supporting SD, HD, “3G” and ASI protocols), DVI input/output, and various other formats. Please contact OmniTek for more information.

**Serial Expansion Ports**
In addition to the Video I/O Module interface, the AVDP also provides two further Serial Expansion connectors. Each supports 4 bidirectional serial I/O channels, and may be connected via flexible PCB links (Samtec Q Pairs™) to additional video expansion I/O modules. Note that the number of additional serial I/O channels is dependent on the choice of main FPGA.

**128Mbit Flash PROM**
The main role of the Flash PROM is to provide the boot code for the Virtex™-5 and Spartan™-3 FPGAs. This code includes the basic PCI-Express interface, to allow flash re-programming and interface control via the PCI-Express interface. Note that the PCB supports up to 512Mbit flash devices.

**Flexible Clock Management**
Frequency synthesis enables clocks for the QDR-II SRAM and DDR2 SDRAM to be individually selected. Alternatively, the memories may be clocked using other frequencies available in the FPGA, for example the primary video clocks. These video clocks are generated at 54.000, 74.250, and 74.176MHz using low-jitter VCXOs and PLL circuits on the AVDP.
PCI Express Controller
This block interfaces with the PCI Express hard macro inside the Virtex™-5 FPGA, to provide the I/O for the control register bus and the DMA controller. It encodes and decodes PCI Express packets into master and slave port I/O according to information stored in the base address registers.

DMA Controller
The DMA Controller allows the on-board SRAM and SDRAM to be accessed from the PCI Express block. Completely autonomous DMA access is achieved using a scatter/gather list previously assembled on the PC. The register set is similar to industry-standard PCI interface DMA controllers.

SDRAM & SRAM Controllers & Video Storage
The SDRAM Controller interfaces to the DDR2 memories. It contains the complete SDRAM state machine, including initialisation and calibration control. The DMA controller directly interfaces to a port on this block. The Video Storage block provides video frame buffer services, as needed for example by the 2D Resizer block. There are equivalent memory controller and video storage blocks for the QDR-II SRAM memories.

Motion Adaptive De-Interlacer
This block performs motion-adaptive de-interlacing of the input video signal. For example, 1080i60 can be converted to 1080p60. Motion is detected by identifying luma and chroma differences between pixels in successive frames, then a decision is made (pixel by pixel) whether to construct the output frame from data in both interlace fields or to interpolate the frame from a single input field. Motion thresholds are user-adjustable.

2D Resizer
The 2D Resizer block delivers accurate resizing and aspect ratio changes between images of arbitrary size. The data width of the image and the number of resampling / low-pass filter taps used by the resizer block can be configured to optimise the trade-off between image quality and IP core size.

Input & Output Blocks
These blocks uses Virtex-5 Multi-Gigabit Transceivers for the Serial Digital Interface inputs and outputs, and all single-link SDTV and HDTV formats are supported in the firmware. (Note that ASI, dual-link and “3G” formats are not supported in the firmware, however the AVDP hardware is fully compatible.) The Input Block contains the SMPTE descrambler, FVH timing reference extraction, and input video format auto-detection. The Output Block contains CRC generation for HD video (or EDH insertion for SD), and the SMPTE output scrambler.

Combiner
This block combines two resized videos and a background video from SRAM into a single video stream in a flexible way, allowing various combinations of “Picture in Picture” and “Picture by Picture” to be configured.

Timing Generator
This block contains control logic to generate all the required synchronization and timing signals to enable the Output Block to create SMPTE-compliant video output signals in the required video format. Note that the AVDP also contains a genlock circuit which can phase-lock the master crystal oscillators to a bi- or tri-level analog sync or serial digital video input; this genlock circuit is controlled by the Spartan-3 FPGA.
The AVDP system comes complete with a Software Development Kit (SDK), including source code in C++ which may be compiled using Microsoft® Visual Studio 2005. The SDK comprises the following items:

Windows® XP or Vista Driver
The AVDP package includes sample 32-bit real-time drivers (compatible with Windows® XP and Vista) to enable efficient interface with the system hardware. Up-to-the-minute industry-standard driver models are used to allow easy adaptation of the existing driver.

Application Programming Interface (API)
As part of the SDK, a fully documented API is provided to enable control of the card in a flexible yet straight-forward manner. Sample Microsoft® DirectShow filters and interface DLLs are provided to demonstrate the design’s flexibility.

Graphical User Interface (GUI)
The SDK contains a sample GUI application that allows speedy access to the hardware features and an example of hardware control via the API and drivers. Features of the GUI include:

- Ability to load and play SD and HD full-motion uncompressed video sequences
- Ability to select between all supported HD and SD video standards
- GUI control of picture resize and de-interlace algorithms
- Live video proxy display of both video input and video output
- Full transport control of SD and HD video sequences being played
- Live video input capture
- Control of I/O re-synchronization module
- Access to low-level hardware registers
- Full memory display & control interface

Documentation
Expansion Connector: 4 x Serial I/O Channels

QDR-II SRAM: 4 x 36Mbit

DDR2 SDRAM: 2 banks x 512MByte (8 chips on reverse)

Virtex-5 FPGA: LX50T, LX110T, SX50T, SX95T

I/O Module Connector: 4 x Serial I/O Channels

VCXOs & PLLs: 54.000, 74.176, 74.250 MHz

Spartan-3 & CoolRunner-II: Boot Control, Housekeeping

PCI Express: x4, x2, or x1

Analog Video Out: YPbPr, RGB, Composite

Card dimensions are 241mm x 111mm ("three-quarter length" PCI-e)
WARRANTY

All equipment is warranted for one year from date of purchase. This includes software and firmware upgrades and hardware repair or replacement, at the discretion of Image Processing Techniques Ltd.

If the hardware is returned to Image Processing Techniques Ltd. for repair, the company cannot be held liable for any loss of stored images or other user data.

THE COMPANY

Image Processing Techniques Ltd. is a consultancy company specializing in the design of products and systems for TV broadcast and post-production applications. Formed in 1998, the company has completed many successful product designs for leading equipment manufacturers in the USA, Europe and Asia.

IPT also designs and manufactures the OmniTek range of advanced test and measurement equipment, for engineers working in video R&D, broadcast, and post-production. The various OmniTek products include signal generators, waveform monitors, and picture quality analyzers. See www.omnitek.tv for more information.

TECHNICAL SPECIFICATIONS

Serial Digital Inputs
Connection 2 x BNC with 75ohm termination
Bit Rates >15dB up to 3GHz
Jitter < 0.2UI, 10Hz to 100kHz

Serial Digital Outputs
Connection 2 x BNC
Bit Rates 270Mbit, 1.485Gbit, 2.97Gbit (SMPTE 259M, 292M, 424M)
Jitter < 0.2UI, 10Hz to 100kHz

Analog Interface
Connection 8-pin Lemo EPG
Video Output RGB with bi- or tri-level sync on green, 0.7Vpk-pk video; or YPbPr with bi- or tri-level sync on Y, 0.7Vpk-pk video; or Composite & S-Video (in PAL or NTSC modes) 0.7Vpk-pk video.
Sync Input 75ohm terminated, return loss >20dB to 30MHz
Black video with bi-level sync (0.3V pk-pk) or tri-level sync (0.6V pk-pk)

Power-Up Time from power-up to serial video output valid: ~1 sec.
Genlock System lock to SDI input or analog sync input.
Output timing adjustable in clock increments from 0 to 1 video frame.

ORDERING INFORMATION

AVDP-LX50T
XC5VLX50T-1 FPGA, 512MByte SDRAM, no SRAM, no analog video.

AVDP-LX110T
XC5VLX110T-1 FPGA, 1GByte SDRAM, 144Mbit SRAM.

AVDP-SX50T
XC5VSX50T-1 FPGA, 512MByte SDRAM, 144Mbit SRAM.

AVDP-SX95T
XC5VXSX95T-1 FPGA, 1GByte SDRAM, 144Mbit SRAM.

AVDP-IO-SDI-2I2O
I/O module with dual SDI/ASI inputs and outputs.

Note 1: All products include software, firmware, and full documentation.
Note 2: All products are RoHS compliant.
Note 3: Please contact OmniTek for information on OEM arrangements or alternative FPGA and memory configurations.