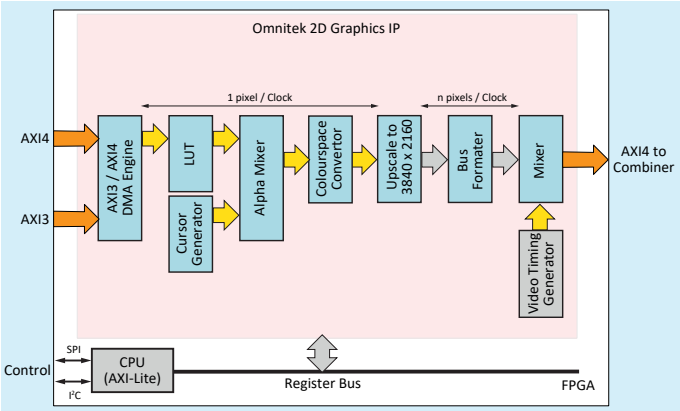
2D Graphics Xilinx FPGA IP

Omnitek

Summary

Omnitek's 2D Graphics IP is a complete solution for adding 2D graphics capability to the Xilinx® Zynq® All Programmable SoCs. This IP allows computer generated 2-dimensional graphics to be rendered as a video frame that can then be overlaid onto a live video stream.

Note that this IP is not necessarily required when using UltraScale Multi-Processor (MP) SoCs devices because these include a Mali GPU that can perform this function.



Functional block diagram of the 2D Graphics IP

The 2D Graphics IP uses three main AXI4 compliant interfaces:

An AXI4-MM interface to connect to the SDRAM

An AXI4-S interface for video output

An AXI4-Lite interface to allow software control

Applications

The 2D Graphics IP can be used in a range of applications including:

- On-screen user interfaces
- Overlay of graphical elements, such as measurements, highlights and warnings on live images.
- Test Pattern Generation
- VR and AR Heads-up displays

Supported Devices

The 2D Graphics IP can be implemented on the following Xilinx devices:

- Artix-7, Kintex-7 and Virtex-7
- Kintex UltraScale and Virtex UltraScale
- Kintex UltraScale+ and Virtex UltraScale+
- Zynq-7000 APSoC and Zynq UltraScale+ MPSoC

Key Features

- Frame Buffer canvas up to 1920x1080 pixels
- Output up to 3840 x 2160
- Support for frame rates up to 120Hz
- Low latency output
- Choice of 16 bits (5:6:5 RGB) or 32 bits (8:8:8:8 RGBA) per pixel
- Configurable Output Colour Matrix
- Dedicated cursor firmware, offloading task of cursor generation from software
- Optional timing generator to allow stand-alone operation (Module output gen-locked to a reference signal via a timing generator)
- Use of AXI4-S for pixel interfaces allows blending of live video with content of Frame Buffer in Omnitek OSD (on-screen display)
- Implementation demonstrated in RTVE reference design.
- Software control of Output Colour Matrix
- Software control of firmware-accelerated cursor
- Linux Frame Buffer driver

Requirements

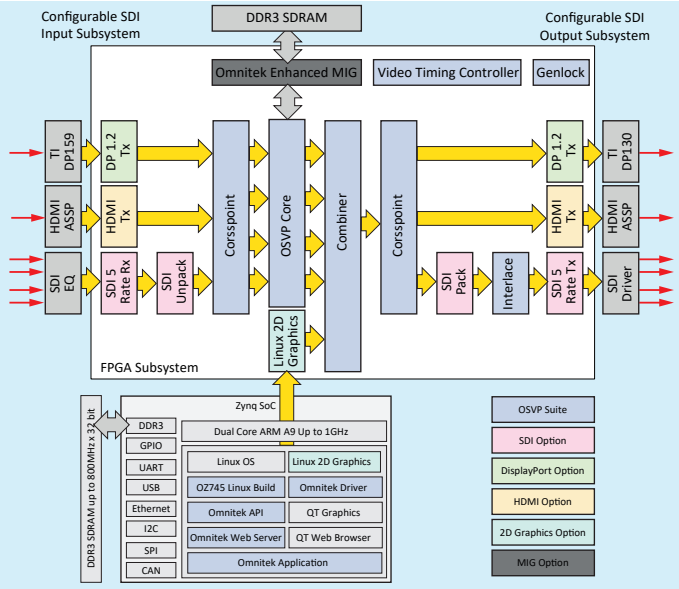
The V-by-One IP requires an ARM processor, MicroBlaze or any AXI4-Lite CPU to allow input / output link configuration.

Connectivity

Omnitek provides a large range of complementary IP Cores for video processing and connection. These IP cores can be used individually or in combination to provide FPGA solutions for applications in broadcast, AV, aerospace/defence, medical, scientific and automotive industries. Omnitek IP Cores can be supplied as discrete blocks for inclusion in your own designs, as single chip solutions or Omnitek can provide a bespoke solution which can be tailored to your specific needs.

RTVE Reference Design

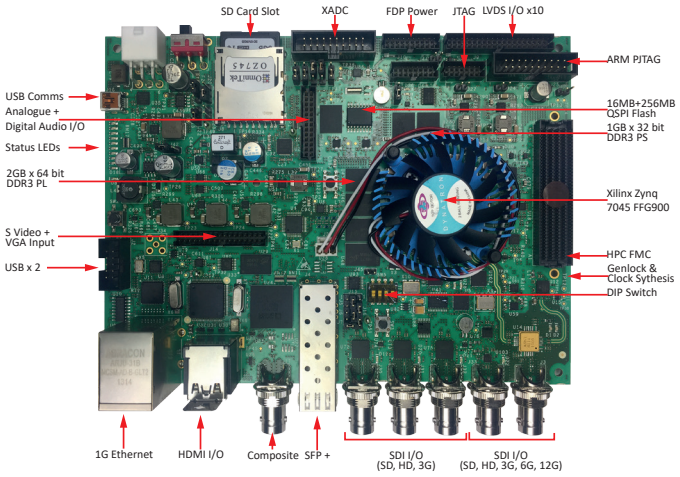
Xilinx's RTVE reference design (Real-Time Video Engine) incorporates a range of IP cores alongside the OSVP Suite (Omnitek Scalable Video Processor) to provide video processing IP and connectivity IP functionality that offers a complete working FPGA design that can be used both to evaluate the performance of the IP blocks in a video application and as a starting point for your own video system designs.



Omnitek OZ745 OSVP Reference Design

Reference Platform

The Omnitek OZ745-3 development platform uses the Xilinx Zynq-XC7Z045-3



Design Environment

All IP blocks optimised for Xilinx FPGA technology

AXI4 memory and control interfaces

Omnitek FPGA Software Interface Framework for easy prototyping, with drivers for Linux, Xilinx Kernel & Windows presenting identical APIs

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About Omnitek

Omnitek is a leading independent consultancy company specializing in the design of video products and IP for the broadcast, post-production, digital film, AV, medical, aerospace/defence, automotive and consumer industries. Since its foundation, Omnitek has completed many successful design projects for major equipment manufacturers throughout Europe, Asia, and the United States.

Omnitek reserves the right to change specifications without notice. Refer to the Omnitek web site for the latest specifications and further information:

www.omnitek.tv

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